

### REMARKS

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the Office Action of April 27, 2005 (hereinafter "Office Action"). In response, Applicants respectfully submit that the cited references do not disclose or suggest, at least, the recitations of the pending independent claims. Accordingly, Applicants submit that all pending claims are in condition for allowance. Favorable reconsideration of all pending claims is respectfully requested for at least the reasons discussed hereafter.

#### **Independent Claim 1 is Patentable**

Independent Claim 1 stands rejected under 35 U.S.C. §102(b) as being anticipated by U. S. Patent No. 6,153,455 to Ling et al. (hereinafter "Ling"). Independent Claim 1 is directed to a method of forming a semiconductor device and recites, in part:

...  
forming spacers on sidewalls of the gate pattern, the spacers having a bottom width;  
implanting impurity ions using the gate pattern and the spacer as a mask to form a heavily doped impurity diffusion layer in the substrate;  
removing the spacers; and  
forming a conformal etch stop layer on the gate pattern and the substrate, wherein the etch stop layer is formed to a thickness of at least the bottom width of the spacers.

Thus, according to independent Claim 1, spacers are formed on sidewalls of the gate pattern and are used as a mask to form a heavily doped impurity diffusion layer. The spacers are removed and an etch stop layer is formed to have a thickness of at least the bottom width of the spacers.

In sharp contrast, Ling describes a method of fabricating a transistor in which a combination of the undoped oxide layer 113 and nitride spacers 134\* form sidewalls spacers that are used as masks during ion implantation as shown in FIGS. 5 and 6. It therefore follows that the undoped oxide layer 113, which serves as an etch stop layer (Ling, col. 6, lines 1 - 2), cannot be formed to a thickness of at least the bottom width of the spacers as recited in Claim 1 because the undoped oxide layer 113 comprises a portion of each spacer.

Thus, as illustrated in FIGS. 4 - 6 of Ling, each spacer is wider than a thickness of the undoped oxide layer 113.

Independent Claim 1 also stands rejected under 35 U.S.C. §102(e) as being anticipated by U. S. Patent No. 6,451,704 to Pradeep et al. (hereinafter "Pradeep"). Pradeep describes oxide spacers that are formed from a silicon dioxide layer 22 (FIGS. 1 and 2). The silicon dioxide layer 22 is described as having a thickness between about 1000 and 5000 Angstroms. (Pradeep, col. 7, lines 58 - 59). The silicon nitride etch stop layer 21 is described as having a thickness of between about 2000 and 3000 Angstroms. (Pradeep, col. 7, line 38). Thus, in sharp contrast with the recitations of Claim 1, Pradeep does not describe or suggest forming the etch stop layer to a thickness of at least the bottom width of the spacers. Rather, Pradeep suggests that the spacers may have a thickness that is greater than the thickness of the etch stop layer 21.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claim 1 is patentable over Ling and Pradeep, either alone or in combination, and that Claims 2 - 11 are patentable at least per the patentability of independent Claim 1.

#### **Independent Claim 12 is Patentable**

Independent Claim 12 stands rejected under 35 U.S.C. §102(e) as being anticipated by Pradeep. Independent Claim 12 is directed to a method of forming a semiconductor device and recites, in part:

...

- forming spacers on sidewalls of the first and second gate patterns, the sidewall spacers having a bottom width;
- forming a heavily doped impurity diffusion layer in the first active region using the first gate pattern and the spacers on the sidewalls of the first gate pattern as a mask;
- removing the spacers; and
- forming a conformal etch stop layer on the first and second gate patterns and the substrate,

wherein the second gate pattern is formed to cross over the device isolation layer and to reach the first active region, and

wherein the etch stop layer is formed to a thickness of at least the

bottom width of the sidewall spacers.

Thus, according to independent Claim 12, spacers are formed on sidewalls of the gate patterns and are used as a mask to form a heavily doped impurity diffusion layer. The spacers are removed and an etch stop layer is formed to have a thickness of at least the bottom width of the spacers.

As discussed above with respect to independent Claim 1, Pradeep describes oxide spacers that are formed from a silicon dioxide layer 22 (FIGS. 1 and 2). The silicon dioxide layer 22 is described as having a thickness between about 1000 and 5000 Angstroms. (Pradeep, col. 7, lines 58 - 59). The silicon nitride etch stop layer 21 is described as having a thickness of between about 2000 and 3000 Angstroms. (Pradeep, col. 7, line 38). Thus, in sharp contrast with the recitations of Claim 12, Pradeep does not describe or suggest forming the etch stop layer to a thickness of at least the bottom width of the spacers. Rather, Pradeep suggests that the spacers may have a thickness that is greater than the thickness of the etch stop layer 21.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claim 12 is patentable over Pradeep, and that Claims 13 - 21 are patentable at least per the patentability of independent Claim 12.

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### CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 on August 29, 2005.



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